Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	95	ECC$1 and (replacement adj processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:44
L2	82733	("707"/$.ccls. or "714"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:34
L3	15070	L2 and (convert$6 or transform$6 or conversion or chang$4) near9 (file or type or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:33
L4	42	1 and (convert$6 or transform$6 or conversion or chang$4) near9 (file or type or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:41
L5	2	4 and ("707"/$.ccls. or "714"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:34
L6	1	4 and (714/710.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:35
L7	469	(714/710.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:35
L8	12	7 and (replacement adj processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:37
L9	11	8 and error and area and (read or reading) and (writing or write or written or wrote)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:40
L10	84	1 and error and area and (read or reading) and (writing or write or written or wrote)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:40

L11	71	1 and error and area and (read or reading) and (writing or write or written or wrote) and sector	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:40
L12	41	11 and (convert$6 or transform$6 or conversion or chang$4) near9 (file or type or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:41
L13	25	11 and (convert$6 or conversion or chang$4) near4 (file or type or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:44
L14	103	((error adj correction adj code) or ECC$1) and (replacement adj processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:44
L15	21	14 and av adj (file or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:45
L16	2	15 and dvd-ram and driver	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:46
L17	2	15 and driver	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:46

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1637	(((error adj correction adj code) or ECC$1) or (replacement adj processing)).ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:49
L2	0	(((error adj correction adj code) or ECC$1) and (replacement adj processing)).ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:58
L3	0	1 and (((error adj correction adj code) or ECC$1) and (replacement adj processing)).ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:44
L4	1058	1 and (((error adj correction adj code) or ECC$1) or (replacement adj processing)).ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:45
L5	2	4 and file adj6 (mode or type)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:44
L6	22	1 and (replacement adj processing). ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:47
L7	14	1 and (replacement adj processing) and error	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:47
L8	0	1 and (replacement adj processing) and error and area and mode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:54
L9	64	(replac$6 near9 (error and area and mode))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:48
L10	0	1 and 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:48

L11	23	9 and (((error adj correction adj code) or ECC$1) or (replacement adj processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:51
L12	1	11 and file adj (type or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:53
L13	1	9 and ((file adj (type or mode)) or ((av or pc) adj (file or mode)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:54
L14	10549	((file adj (type or mode)) or ((av or pc) adj (file or mode)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:00
L15	6	14 and (replacement adj processing) and error and area and mode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:58
L16	110	(replacement adj processing) and error and area and mode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:58
L17	49	16 and (((error adj correction adj code) or ECC$1) and (replacement adj processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:01
L18	5	17 and ((av or pc) adj (file or mode))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 12:59
L19	6	17 and ((file adj (type or mode)) or ((av or pc) adj (file or mode)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:01
L20	15968	((file adj2 (type or mode)) or ((av or pc) adj (file or mode)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:19

L21	22	20 and (((error adj correction adj code) or ECC$1) and (replacement adj processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:08
L22	3211	20 and ("707"/$.ccls. or "714"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:08
L23	96	22 and (((error adj correction adj code) or ECC$1) or (replacement adj processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:20
L24	68	23 and sector	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:20
L25	67	24 and (read or reading) and writ$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:17
L26	65	24 and (read and reading) and writ$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:10
L27	59	24 and (read and reading) and write and writing and written	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:21
L28	20399	((file adj2 (type or mode)) or ((av or pc) adj (file or mode or data)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:19
L29	25659	((file adj2 (type or mode)) or ((av or pc) adj2 (file or mode or data)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:19
L30	26	28 and (((error adj correction adj code) or ECC$1) and (replacement adj processing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:20

L31	23	30 and sector	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:20
L32	20	31 and (read and reading) and write and writing and written	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:23
L33	25	30 and (convert$6 or transform$6 or conversion or chang$5) near6 (data or information or av or pc or mode or file or type)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 13:24

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	63	ECC$1 and error and (replacement adj processing) and recording and recorded and ((recording adj area) or sector)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:49
L2	6	1 and (dvd-ram and driver)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:42
L3	63	1 and (convert$6 or conversion or transform$6 or translat$6 or replac$9)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:44
L4	45	1 and (convert$6 or conversion or transform$6 or translat$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:50
L5	1	1 and (pc and av) adj2 (type or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:45
L6	20	(pc and av) adj2 (type or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:45
L7	0	(pc and av) adj2 (type and mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:45
L9	17	(pc and av) adj2 (file\ and mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:45
L10	1	(pc and av) adj2 (file and mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:45
L11	17	(pc and av) adj2 mode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:46

L12	91	ECC$1 and error and (replacement adj processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:54
L13	11	12 and (convert$6 or conversion or transform$6 or translat$6) with file	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:52
L14	17253	(error adj correction adj code)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:59
L15	7131	14 and error with (read or reading or writ$4 or written)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:53
L16	1182	14 and (data adj error) with (read or reading or writ$4 or written)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:54
L17	597	14 and (data adj error) adj9 (read or reading or writ$4 or written)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:01
L18	12	17 and ECC$1 and error and (replacement adj processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:58
L19	10	18 and file	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:56
L20	10	18 and file and type	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:56
L21	15	14 and ECC$1 same error same (replacement adj processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:58

L22	20	14 and ((error adj correction adj code) or ECC$1) same error same (replacement adj processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:59
L23	13	22 and (data adj error) and (read or reading) and (writ$4 or written)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:03
L24	13	23 and file and dvd-ram	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:03
S1	1087	(ECC adj blocks!)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:30
S2	197	S1 and ("707"/$.ccls. or "714"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 13:50
S3	22	S2 and file adj type	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 13:42
S4	1570	(ECC adj block) and sector	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 13:49
S5	1	S4 and (convert$6 or transform$6 or conversion) with (file adj3 (type or mode))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 13:48
S6	1	S1 and (convert$6 or transform$6 or conversion) with (file adj3 (type or mode))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 13:48
S7	812	(convert$6 or transform$6 or conversion) with (file adj3 (type or mode))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 13:50

S8	152	S7 and ("707"/$.ccls. or "714"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 13:49
S9	1	S8 and ECC and sector	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 13:49
S10	3	S8 and ECC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 13:49
S11	82566	("707"/$.ccls. or "714"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 13:50
S12	152	S11 and (convert$6 or transform$6 or conversion) with (file adj3 (type or mode))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 13:51
S13	17	S12 and recording adj medium	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 15:43
S14	2	"5270957".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 15:44
S15	10	("20030120593" or "20040064443" or "6208990" "6189004" or "6151608"). pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 06:30
S16	2	"5270957".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 06:50
S17	2	S16 and distribution	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 06:51

S18	2	S16 and distribution and replac$8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 06:57
S19	2	S16 and distribution and replac$8 and probabilit$7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 07:04
S20	1	S16 and binomial	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 07:06
S21	0	S16 and (weight$4 or scor$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 07:06

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	63	ECC$1 and error and (replacement adj processing) and recording and recorded and ((recording adj area) or sector)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:49
L2	6	1 and (dvd-ram and driver)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:42
L3	63	1 and (convert$6 or conversion or transform$6 or translat$6 or replac$9)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:44
L4	45	1 and (convert$6 or conversion or transform$6 or translat$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:50
L5	1	1 and (pc and av) adj2 (type or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:45
L6	20	(pc and av) adj2 (type or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:45
L7	0	(pc and av) adj2 (type and mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:45
L9	17	(pc and av) adj2 (file\ and mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:45
L10	1	(pc and av) adj2 (file and mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:45
L11	17	(pc and av) adj2 mode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:46

L12	91	ECC$1 and error and (replacement adj processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:54
L13	11	12 and (convert$6 or conversion or transform$6 or translat$6) with file	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:52
L14	17253	(error adj correction adj code)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:59
L15	7131	14 and error with (read or reading or writ$4 or written)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:53
L16	1182	14 and (data adj error) with (read or reading or writ$4 or written)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:54
L17	597	14 and (data adj error) adj9 (read or reading or writ$4 or written)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:01
L18	12	17 and ECC$1 and error and (replacement adj processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:58
L19	10	18 and file	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:56
L20	10	18 and file and type	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:56
L21	15	14 and ECC$1 same error same (replacement adj processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:58

L22	20	14 and ((error adj correction adj code) or ECC$1) same error same (replacement adj processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 10:59
L23	13	22 and (data adj error) and (read or reading) and (writ$4 or written)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:03
L24	13	23 and file and dvd-ram	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:03

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	95	ECC$1 and (replacement adj processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:35
L2	82733	("707"/$.ccls. or "714"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:34
L3	15070	L2 and (convert$6 or transform$6 or conversion or chang$4) near9 (file or type or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:33
L4	42	1 and (convert$6 or transform$6 or conversion or chang$4) near9 (file or type or mode)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:34
L5	2	4 and ("707"/$.ccls. or "714"/$.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:34
L6	1	4 and (714/710.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:35
L7	469	(714/710.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:35
L8	12	7 and (replacement adj processing)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:37
L9	11	8 and error and area and (read or reading) and (writing or write or written or wrote)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/02 11:38

Terms used replacement processing error ecc

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Relevance scale

1 Features: Self-healing in modern operating systems
Michael W. Shapiro
December 2004 **Queue**, Volume 2 Issue 9
Publisher: ACM Press
Full text available: pdf(872.84 KB) html(32.65 KB)
Additional Information: full citation, abstract, references, index terms

A few early steps show there's a long (and bumpy) road ahead.

2 The Wisconsin Wind Tunnel: virtual prototyping of parallel computers
Steven K. Reinhardt, Mark D. Hill, James R. Larus, Alvin R. Lebeck, James C. Lewis, David A. Wood
June 1993 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1993 ACM SIGMETRICS conference on Measurement and modeling of computer systems SIGMETRICS '93**, Volume 21 Issue 1
Publisher: ACM Press
Full text available: pdf(1.40 MB)
Additional Information: full citation, abstract, references, citings, index terms

We have developed a new technique for evaluating cache coherent, shared-memory computers. The Wisconsin Wind Tunnel (WWT) runs a parallel shared-memory program on a parallel computer (CM-5) and uses execution-driven, distributed, discrete-event simulation to accurately calculate program execution time. WWT is a virtual prototype that exploits similarities between the system under design (the target) and an existing evaluation platform (the host). The host directly executes all target program ins ...

3 Trap-driven memory simulation with Tapeworm II
Richard Uhlig, David Nagle, Trevor Mudge, Stuart Sechrest
January 1997 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 7 Issue 1
Publisher: ACM Press
Full text available: pdf(630.91 KB)
Additional Information: full citation, references, index terms

Keywords: Cache, TLB, memory system, simulation, trace-driven simulation, trap-driven simulation

4 Trace-driven memory simulation: a survey
Richard A. Uhlig, Trevor N. Mudge
June 1997 **ACM Computing Surveys (CSUR)**, Volume 29 Issue 2
Publisher: ACM Press
Full text available: pdf(636.11 KB) Additional Information: full citation, abstract, references, citings, index terms, review

As the gap between processor and memory speeds continues to widen, methods for evaluating memory system designs before they are implemented in hardware are becoming increasingly important. One such method, trace-driven memory simulation, has been the subject of intense interest among researchers and has, as a result, enjoyed rapid development and substantial improvements during the past decade. This article surveys and analyzes these developments by establishing criteria for evaluating trac ...

Keywords: TLBs, caches, memory management, memory simulation, trace-driven simulation

5 Parameter replacement for CELP coded speech in land mobile radio
Yaacov Yesha
July 1998 **Wireless Networks**, Volume 4 Issue 4
Publisher: Kluwer Academic Publishers
Full text available: pdf(90.72 KB) Additional Information: full citation, abstract, references, index terms

The contribution of this paper is in applying parameter replacement techniques to speech that is compressed by the Federal Standard 1016 CELP speech coder, protected by Reed-Solomon codes, and transmitted over a wireless channel. The parameter replacement results in significant improvement in speech quality without any increase in bit rate.

6 Assessing Fault Sensitivity in MPI Applications
Charng-da Lu, Daniel A. Reed
November 2004 **Proceedings of the 2004 ACM/IEEE conference on Supercomputing**
Publisher: IEEE Computer Society
Full text available: pdf(678.48 KB) Additional Information: full citation, abstract

Today, clusters built from commodity PCs dominate high-performance computing, with systems containing thousands of processors now being deployed. As node counts for multi-teraflop systems grow to thousands and with proposed petaflop system likely to contain tens of thousands of nodes, the standard assumption that system hardware and software are fully reliable becomes much less credible. Concomitantly, understanding application sensitivity to system failures is critical to establishing confidenc ...

7 Trap-driven simulation with Tapeworm II
Richard Uhlig, David Nagle, Trevor Mudge, Stuart Sechrest
November 1994 **ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the sixth international conference on Architectural support for programming languages and operating systems ASPLOS-VI**, Volume 29 , 28 Issue 11 , 5
Publisher: ACM Press
Full text available: pdf(1.45 MB) Additional Information: full citation, abstract, references, citings, index terms

Tapeworm II is a software-based simulation tool that evaluates the cache and TLB performance of multiple-task and operating system intensive workloads. Tapeworm resides in an OS kernel and causes a host machine's hardware to drive simulations with kernel traps instead of with address traces, as is conventionally done. This allows Tapeworm to quickly and accurately capture complete memory referencing behavior with

a limited degradation in overall system performance. This paper compares trap- ...

Keywords: TLB, cache, memory system, trace-driven simulation, trap-driven simulation

8 Active memory: a new abstraction for memory system simulation
Alvin R. Lebeck, David A. Wood
January 1997 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 7 Issue 1
Publisher: ACM Press
Full text available: pdf(690.38 KB) Additional Information: full citation, references, citings, index terms

Keywords: Cache memory, direct-execution simulation, memory hierarchy, on-the-fly simulation, trace-driven simulation

9 Survey of software tools for evaluating reliability, availability, and serviceability
Allen M. Johnson, Miroslaw Malek
September 1988 **ACM Computing Surveys (CSUR)**, Volume 20 Issue 4
Publisher: ACM Press
Full text available: pdf(3.79 MB) Additional Information: full citation, abstract, references, citings, index terms

In computer design, it is essential to know the effectiveness of different design options in improving performance and dependability. Various software tools have been created to evaluate these parameters, applying both analytic and simulation techniques, and this paper reviews those related primarily to reliability, availability, and serviceability. The purpose, type of models used, type of systems modeled, inputs, and outputs are given for each package. Examples of some of the key modeling ...

10 Selective-set-invalidation (SSI) for soft-error-resilient cache architecture
Seung H. Hwang, Gwan S. Choi
June 1999 **ACM SIGARCH Computer Architecture News**, Volume 27 Issue 3
Publisher: ACM Press
Full text available: pdf(489.77 KB) Additional Information: full citation, abstract, index terms

This paper proposes a novel cache-memory design for soft-error silence, and verifies the design through a simulation that uses realistic system and software model. The SSI design is a combination of an n-bit error detector and a fast circuit that allows real-time-forced invalidation of corrupted data sets. The current design supports the write through caching policy and will be extended for the write back policy. To verify the effectiveness of the proposed design approach, mixed-mode simulations ...

11 Area efficient architectures for information integrity in cache memories
Seongwoo Kim, Arun K. Somani
May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture ISCA '99**, Volume 27 Issue 2
Publisher: IEEE Computer Society, ACM Press
Full text available: pdf(227.09 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Information integrity in cache memories is a fundamental requirement for dependable computing. Conventional architectures for enhancing cache reliability using check codes make it difficult to trade between the level of data integrity and the chip area

requirement. We focus on transient fault tolerance in primary cache memories and develop new architectural solutions, to maximize fault coverage when the budgeted silicon area is not sufficient for the conventional configuration of an error checki ...

12 RAID: high-performance, reliable secondary storage
Peter M. Chen, Edward K. Lee, Garth A. Gibson, Randy H. Katz, David A. Patterson
June 1994 **ACM Computing Surveys (CSUR)**, Volume 26 Issue 2
Publisher: ACM Press
Full text available: pdf(3.60 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Disk arrays were proposed in the 1980s as a way to use parallelism between multiple disks to improve aggregate I/O performance. Today they appear in the product lines of most major computer manufacturers. This article gives a comprehensive overview of disk arrays and provides a framework in which to organize current and future work. First, the article introduces disk technology and reviews the driving forces that have popularized disk arrays: performance and reliability. It discusses the tw ...

Keywords: RAID, disk array, parallel I/O, redundancy, storage, striping

13 Evolutionary computation and optimization (ECO): Solving the error correcting code problem with parallel hybrid heuristics
Enrique Alba, J. Francisco Chicano
March 2004 **Proceedings of the 2004 ACM symposium on Applied computing**
Publisher: ACM Press
Full text available: pdf(289.83 KB) Additional Information: full citation, abstract, references, index terms

Some telecommunication systems can not afford the cost of repeating a corrupted message. Instead, the message should be somewhat "corrected" by the receiver. In these cases an *error correcting code* is suitable. The problem of finding an error correcting code of *n* bits and *M* codewords that corrects a given maximum number of errors is NP-hard. For this reason the problem has been solved in the literature with heuristic techniques such as Simulated Annealing and Genetic Algorit ...

Keywords: heuristics, information theory, local search, parallelism

14 Efficient checker processor design
Saugata Chatterjee, Chris Weaver, Todd Austin
December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**
Publisher: ACM Press
Full text available: pdf(153.00 KB)
ps(1.26 MB) Additional Information: full citation, references, citings, index terms
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15 A proof of the security of quantum key distribution (extended abstract)
Eli Biham, Michel Boyer, P. Oscar Boykin, Tal Mor, Vwani Roychowdhury
May 2000 **Proceedings of the thirty-second annual ACM symposium on Theory of computing**
Publisher: ACM Press
Full text available: pdf(968.70 KB) Additional Information: full citation, references, citings, index terms

16 DIVA: a reliable substrate for deep submicron microarchitecture design
Todd M. Austin
November 1999 **Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture**
Publisher: IEEE Computer Society
Full text available: pdf(1.47 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Building a high-performance microprocessor presents many reliability challenges. Designers must verify the correctness of large complex systems and construct implementations that work reliably in varied (and occasionally adverse) operating conditions. To further complicate this task, deep submicron fabrication technologies present new reliability challenges in the form of degraded signal quality and logic failures caused by natural radiation interference.

17 Execution-driven simulation of multiprocessors: address and timing analysis
S. Dwarkadas, J. R. Jump, J. B. Sinclair
October 1994 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 4 Issue 4
Publisher: ACM Press
Full text available: pdf(1.58 MB) Additional Information: full citation, abstract, references, citings, index terms

This article describes and evaluates an efficient execution-driven technique for the simulation of multiprocessors that includes the simulation of system memory and that is driven by real program work loads. The technique produces correctly interleaved address traces at run-time without disk access overhead or hardware support, allowing accurate simulation of the effects of a variety of architectural alternatives on programs. We have implemented a simulator based on this technique that offe ...

Keywords: distributed systems, execution-driven simulation, parallel tracing, shared-memory multiprocessors

18 Piranha: a scalable architecture based on single-chip multiprocessing
Luiz André Barroso, Kourosh Gharachorloo, Robert McNamara, Andreas Nowatzyk, Shaz Qadeer, Barton Sano, Scott Smith, Robert Stets, Ben Verghese
May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture ISCA '00**, Volume 28 Issue 2
Publisher: ACM Press
Full text available: pdf(191.10 KB) Additional Information: full citation, abstract, references, citings, index terms

The microprocessor industry is currently struggling with higher development costs and longer design times that arise from exceedingly complex processors that are pushing the limits of instruction-level parallelism. Meanwhile, such designs are especially ill suited for important commercial applications, such as on-line transaction processing (OLTP), which suffer from large memory stall times and exhibit little instruction-level parallelism. Given that commercial applications constitute by fa ...

19 Evaluating the memory overhead required for COMA architectures
T. Joe, J. L. Hennessy
April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture ISCA '94**, Volume 22 Issue 2

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(1.31 MB) Additional Information: full citation, abstract, references, citings, index terms

Cache only memory architectures (COMA) have an inherent memory overhead due to the organization of main memory as a large cache called an attraction memory. This overhead consists of memory left unallocated for performance reasons as well as additional physical memory required due to the cache organization of memory. In this work, we examine the effect of data reshuffling and data replication on the memory overhead. Data reshuffling occurs when space needs to be allocated to store a remote memor ...

20 General storage protection techniques: Ensuring data integrity in storage: techniques and applications

Gopalan Sivathanu, Charles P. Wright, Erez Zadok

November 2005 **Proceedings of the 2005 ACM workshop on Storage security and survivability StorageSS '05**

Publisher: ACM Press

Full text available: pdf(217.83 KB) Additional Information: full citation, abstract, references, index terms

Data integrity is a fundamental aspect of storage security and reliability. With the advent of network storage and new technology trends that result in new failure modes for storage, interesting challenges arise in ensuring data integrity. In this paper, we discuss the causes of integrity violations in storage and present a survey of integrity assurance techniques that exist today. We describe several interesting applications of storage integrity checking, apart from security, and discuss the im ...

Keywords: file systems, intrusion detection, storage integrity

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1 Error correcting codes, perfect hashing circuits, and deterministic dynamic dictionaries
Peter Bro Miltersen
January 1998 **Proceedings of the ninth annual ACM-SIAM symposium on Discrete algorithms**
Publisher: Society for Industrial and Applied Mathematics
Full text available: pdf(1.01 MB) Additional Information: full citation, references, citings, index terms

2 Linear-time encodable and decodable error-correcting codes
Daniel A. Spielman
May 1995 **Proceedings of the twenty-seventh annual ACM symposium on Theory of computing**
Publisher: ACM Press
Full text available: pdf(993.36 KB) Additional Information: full citation, references, citings, index terms

3 Error-correcting codes for semiconductor memories
C. L. Chen
January 1984 **ACM SIGARCH Computer Architecture News , Proceedings of the 11th annual international symposium on Computer architecture ISCA '84,** Volume 12 Issue 3
Publisher: ACM Press
Full text available: pdf(242.74 KB) Additional Information: full citation, references, index terms

4 Multiclass learning, boosting, and error-correcting codes
Venkatesan Guruswami, Amit Sahai
July 1999 **Proceedings of the twelfth annual conference on Computational learning theory**
Publisher: ACM Press
Full text available: pdf(1.30 MB) Additional Information: full citation, references, citings, index terms

5

On the efficiency of local decoding procedures for error-correcting codes
Jonathan Katz, Luca Trevisan
May 2000 **Proceedings of the thirty-second annual ACM symposium on Theory of computing**
Publisher: ACM Press
Full text available: pdf(732.43 KB) Additional Information: full citation, references, citings, index terms

6 Using a genetic algorithm to find good linear error-correcting codes
Kelly M. McGuire, Roberta Evans Sabin
February 1998 **Proceedings of the 1998 ACM symposium on Applied Computing**
Publisher: ACM Press
Full text available: pdf(470.83 KB) Additional Information: full citation, references, index terms

Keywords: genetic algorithm, linear error correcting codes

7 Declustering using error correcting codes
C. Faloutsos, D. Metaxas
March 1989 **Proceedings of the eighth ACM SIGACT-SIGMOD-SIGART symposium on Principles of database systems**
Publisher: ACM Press
Full text available: pdf(616.35 KB) Additional Information: full citation, abstract, references, citings, index terms

The problem examined is to distribute a binary Cartesian product file on multiple disks to maximize the parallelism for partial match queries. Cartesian product files appear as a result of some secondary key access methods, such as the multiattribute hashing [10], the grid file [6] etc.. For the binary case, the problem is reduced into grouping the 2n binary strings on n bits in m groups of unsimilar strings. The main i ...

8 Evolutionary computation and optimization (ECO): Solving the error correcting code problem with parallel hybrid heuristics
Enrique Alba, J. Francisco Chicano
March 2004 **Proceedings of the 2004 ACM symposium on Applied computing**
Publisher: ACM Press
Full text available: pdf(289.83 KB) Additional Information: full citation, abstract, references, index terms

Some telecommunication systems can not afford the cost of repeating a corrupted message. Instead, the message should be somewhat "corrected" by the receiver. In these cases an *error correcting code* is suitable. The problem of finding an error correcting code of *n* bits and *M* codewords that corrects a given maximum number of errors is NP-hard. For this reason the problem has been solved in the literature with heuristic techniques such as Simulated Annealing and Genetic Algorit ...

Keywords: heuristics, information theory, local search, parallelism

9 A fuzzy commitment scheme
Ari Juels, Martin Wattenberg
November 1999 **Proceedings of the 6th ACM conference on Computer and communications security**
Publisher: ACM Press

Full text available: pdf(966.08 KB) Additional Information: full citation, abstract, references, citings, index terms

We combine well-known techniques from the areas of error-correcting codes and cryptography to achieve a new type of cryptographic primitive that we refer to as a fuzzy commitment scheme. Like a conventional cryptographic commitment scheme, our fuzzy commitment scheme is both concealing and binding: it is infeasible for an attacker to learn the committed value, and also for the committer to decommit a value in more than one way. In a convent ...

10 Cryptanalysis of private-key encryption schemes based on burst-error-correcting codes
Hung-Min Sun, Shiuh-Pyng Shieh
January 1996 **Proceedings of the 3rd ACM conference on Computer and communications security**
Publisher: ACM Press
Full text available: pdf(329.04 KB) Additional Information: full citation, references, index terms

11 Faster solution of the key equation for decoding BCH error-correcting codes
Victor Y. Pan
May 1997 **Proceedings of the twenty-ninth annual ACM symposium on Theory of computing**
Publisher: ACM Press
Full text available: pdf(1.15 MB) Additional Information: full citation, references, index terms

12 Performance analysis of DS-CDMA with slotted ALOHA random access for packet PCNs
Zhao Liu, Magda El Zarki
February 1995 **Wireless Networks**, Volume 1 Issue 1
Publisher: Kluwer Academic Publishers
Full text available: pdf(1.56 MB) Additional Information: full citation, abstract, references, citings, index terms, review

In this paper, we present a discrete time Markov chain based analytical framework for the study of Direct-Sequence Code-Division-Multiple-Access (DS-CDMA) with slotted ALOHA random access protocols (DS-CDMA-S-ALOHA) for packet Personal Communications Networks (PCNs). It incorporates both the random access and the random errors associated with DS-CDMA-S-ALOHA protocols into a unified framework. The key feature is that it distinguishes between the two stages in the transmission process, namel ...

13 Session 8 (brief announcements): Asynchronous interactive consistency and its relation with error-correcting codes
Achour Mostefaoui, Sergio Rajsbaum, Michel Raynal
July 2002 **Proceedings of the twenty-first annual symposium on Principles of distributed computing**
Publisher: ACM Press
Full text available: pdf(102.60 KB) Additional Information: full citation, references

14 Complexity theory: Guest column: error-correcting codes and expander graphs
Venkatesan Guruswami
September 2004 **ACM SIGACT News**, Volume 35 Issue 3

Publisher: ACM Press
Full text available: pdf(650.42 KB) Additional Information: full citation, abstract, references

The central algorithmic problem in coding theory is the construction of explicit error-correcting codes with good parameters together with fast algorithms for encoding a message and decoding a noisy received word into the correct message. Over the last decade, significant new developments have taken place on this problem using graph-based/combinatorial constructions that exploit the power of <i>expander graphs</i>. The role of expander graphs in theoretical computer science is by now ...

15 Extractors and pseudorandom generators
July 2001 **Journal of the ACM (JACM)**, Volume 48 Issue 4
Publisher: ACM Press
Full text available: pdf(181.64 KB) Additional Information: full citation, abstract, references, citings, index terms, review

We introduce a new approach to constructing extractors. Extractors are algorithms that transform a "e;weakly random"e; distribution into an almost uniform distribution. Explicit constructions of extractors have a variety of important applications, and tend to be very difficult to obtain.We demonstrate an unsuspected connection between extractors and pseudorandom generators. In fact, we show that every pseudorandom generator of a certain kind is an extractor.A pseudorandom generator const ...

Keywords: Error-correcting codes, extractors, pseudorandomness

16 Declustering of key-based partitioned signature files
Paolo Ciaccia, Paolo Tiberio, Pavel Zezula
September 1996 **ACM Transactions on Database Systems (TODS)**, Volume 21 Issue 3
Publisher: ACM Press
Full text available: pdf(2.58 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Access methods based on signature files can largely benefit from possibilities offered by parallel environments. To this end, an effective declustering strategy that would distribute signatures over a set of parallel independent disks has to be combined with a synergic clustering which is employed to avoid searching the whole signature file while executing a query. This article proposes two parallel signature file organizations, Hamming Filter (HF
Keywords: error correcting codes, information retrieval, parallel independent disks, partial match queries, performance evaluation, superimposed coding

17 Extracting all the randomness and reducing the error in Trevisan's extractors
Ran Raz, Omer Reingold, Salil Vadhan
May 1999 **Proceedings of the thirty-first annual ACM symposium on Theory of computing**
Publisher: ACM Press
Full text available: pdf(870.20 KB) Additional Information: full citation, references, citings, index terms

18 Session 11A: Extractors: optimal up to constant factors
Chi-Jen Lu, Omer Reingold, Salil Vadhan, Avi Wigderson
June 2003 **Proceedings of the thirty-fifth annual ACM symposium on Theory of computing**
Publisher: ACM Press

Full text available: pdf(246.08 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper provides the first explicit construction of extractors which are simultaneously optimal up to constant factors in *both* seed length and output length. More precisely, for every *n,k*, our extractor uses a random seed of length *O(log n)* to transform any random source on *n* bits with (min-)entropy *k*, into a distribution on *(1-α)k* bits that is ε-close to uniform. Here *α* and ε can be taken to be any positive c ...

Keywords: condensers, locally decodable error-correcting codes, mergers, pseudorandomness, randomness extractors

19 Distributed fingerprints and secure information dispersal
Hugo Krawczyk
September 1993 **Proceedings of the twelfth annual ACM symposium on Principles of distributed computing**
Publisher: ACM Press
Full text available: pdf(1.03 MB) Additional Information: full citation, references, citings, index terms

20 Error-resilient transmission of 3D models
Ghassan Alregib, Yucel Altunbasak, Jarek Rossignac
April 2005 **ACM Transactions on Graphics (TOG)**, Volume 24 Issue 2
Publisher: ACM Press
Full text available: pdf(10.73 MB) Additional Information: full citation, abstract, references, index terms

In this article, we propose an error-resilient transmission method for progressively compressed 3D models. The proposed method is scalable with respect to both channel bandwidth and channel packet-loss rate. We jointly design source and channel coders using a statistical measure that (i) calculates the number of both source and channel coding bits, and (ii) distributes the channel coding bits among the transmitted refinement levels in order to maximize the expected decoded model quality. In orde ...

Keywords: 3D graphics compression, error resilience, joint source and channel coding, media streaming, priority encoding transmission, progressive transmission, unequal error protection, virtual reality over IP

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Global Telecommunications Conference, 1999. GLOBECOM '99
Volume 1B, 1999 Page(s):749 - 754 vol. 1b
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Volume 31, Issue 2, Mar 1995 Page(s):1044 - 1049

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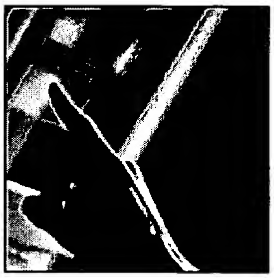

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Science Dynamics Corporation (Cherry Hill, NJ)

Summary:

A BMDO SBIR Phase I contract for virtual memory redundancy management has led to an error-correction code (ECC) for data transmission systems that are more efficient than current methods in use. ECCs are used in all forms of digital circuitry and communications, from CD players to satellite links. The ECC was originally developed by GORCA Systems Incorporated (GSI; Cherry Hill, NJ) and then used as the basis for the formation of GORCA Memory Systems, Inc. (GMS; Cherry Hill, NJ). In 1999 that version of the ECC was purchased by Science Dynamics Corporation (SIDY; Cherry Hill, NJ). The ECC has since been enhanced by a combination of engineering efforts from SIDY and Technology Enhancement Partners, LLC (TEP; Medford, NJ). The first product of this joint effort is to be packaged in an error-correction chip for use in wireless local area networks and marketed by SIDY. Additional products are being developed by SIDY and TEP together and separately.

Technology Description:

In the mid 1990s, GORCA Memory Systems (GMS; Cherry Hill, NJ) was formed to create and market products using an error-correction code (ECC) that was developed by Walter Helbig, a consultant to GORCA Systems Incorporated (GSI; Cherry Hill, NJ). The system was purchased by Science Dynamics Corporation (SIDY; Cherry Hill, NJ) when GMS went out of business. SIDY and Technology Enhancement Partners, LLC (TEP; Cherry Hill, NJ) are jointly refining the ECC and developing new products and applications using it.

Error correcting is essential for error-free transmission of digital data. Whenever one digital component is tasked with sending bits to a second component (a "component" may be any digital device such as a cellular phone, computer network card, or computer memory that transmits data to the computer's processor), the possibility

for the data set becoming corrupted in route arises. Error correction is made available by adding checksum bits to the packets of data that move between components. These bits allow the receiving component to determine if the packet of data arrived intact. Unfortunately, checksum bits also add overhead to each data packet ("overhead" is the percentage of checksum bits to data bits per packet). The larger the overhead, the lengthier the packets, and, therefore, the longer it takes for the entire set of data to be transmitted.

GMS's patented ECC is a form of a computable rotational code that can operate as a single burst-error correcting, multiple burst-error detecting code. Whereas most industry standard schemes, such as the Reed-Solomon (RS) code, operate at a fixed symbol length and, in typical implementations require an overhead of approximately eight percent, this code is designed to operate in the same applications with a much smaller overhead, typically on the order of one percent. The arithmetic process used with this code is similar to that used in the National Security Agency's secure hash algorithm (SHA-1). As such, the computational rate is much higher than it is for the RS code while the cost of implementation is anticipated to be considerably less. Further, the code provides modification correction capability in addition to modification detection capability at costs approximately equal to that of the SHA-1 code. Because there are virtually an infinite number of variations to this code, users can implement the single version or multiple versions that optimally match the intended application.

This ECC can facilitate further efficiency in virtual memory-addressing settings, because part of the ECC can be implemented on the virtual memory translation unit itself. Plus, because of its compact design, this code can be implemented on a single field-programmable gate array, which is a type of programmable logic chip, thereby saving production costs over error-correcting schemes that require more elaborate hardware.

BMD Origins:

In 1992, GSI completed a BMDO SBIR Phase I on virtual memory redundancy management for reliable multiprocessing. BMDO needed to facilitate complex, low-error rate data communications between satellite and ground systems. The original design was for a block-error correction for high-capacity, high-performance, solid-state memory systems.

Spinoff Applications:

Although error corrections are used in all forms of digital circuitry, from CD players to computers, efficient error correction is particularly valued in wireless communications, where throughput is already more limited than land-based lines. So everything from satellite communication links to cell phones could benefit from efficient error correction.

One possible application is in wireless local area networks (WLANs). These are similar to office networks of computers but, instead of the computers being attached to one another by cables, they communicate by radio signals. WLANS are useful for companies in old buildings where cable installation is costly or prohibitive. They might also be used with offices that are mobile. According to the Cahners In-Stat Group research firm, the corporate WLAN market may be worth $2.2 billion by 2004.

Another application area is in digital signatures. A digital signature is code that identifies the sender of an electronic document. Digital signatures were created to provide the electronic equivalent to written signatures. That is to say, they can guarantee the identity of the signer of the document. Because of this, digital signatures are predicted to become a cornerstone of the e-commerce marketplace, which requires authentication to conduct business. This ECC can be used in a digital signature system and can provide an additional benefit of error-correcting documents as they are transmitted.

Commercialization:

The present version of the error-detecting and correcting system is now jointly owned by SIDY and TEP. The first product that employs the technology is a forward error-correcting (FEC) chip that SIDY is now marketing. GMS' principal investigator Walter Helbig, who founded TEP, is making further improvements to the ECC for applications for both companies.

SIDY and TEP have designed the forward error correcting (FEC) chip using this technology, called HSBC (Helbig-Shrinivasan Block Code) Burst Error Detection and Correction (HEDCtm). This chip could be used in commercial satellite terminals to replace the larger, more expensive, and less efficient Reed-Solomon FEC (which has about an eight-percent communication overhead).

TE is proposing that the HEDC chip (or variants of it) be accepted by the IEEE 802 standards bodies for the newer communications systems. The value of this code and its implementation can be seen in that in a typical WLAN one in every 100,000 packets transmitted will be received with errors. SIDY and TEP have shown that HEDC can, in this application, correct all these errors. Plus, they have shown that the HEDC chip is less costly than the Reed-Solomon components for the same system, as its efficient design can be implemented entirely on one integrated circuit. SIDY estimates that its HEDC chip will cost approximately a tenth of the full set of components for the Reed-Solomon unit. The HEDC FEC chip can work either in half-duplex or full-duplex mode, and has a capability of over 20 megabits per second, with gigabyte-level throughput possible. Further, the HEDC chip can automatically switch between handling short command packets (of up to 512 data bytes in length) and longer information packets (of over 512 data bytes in length).

SIDY may also employ the ECC in the global telecommunications network being built by SIDY for Cascadent Communications, Ltd. (Washington, D.C.). SIDY is a supplier of key technologies to this company, which has an ambitious plan for building a seamless Internet protocol-based global communications facility for large to medium corporate users with international communications requirements.

TEP is working toward employing the ECC as a part of secure computer systems. It is working with the McLean, VA-based Amron Corporation on an SBIR Phase I contract for the Navy SPAWAR program. The work involves the creation of a Security Level B-2 computer design. The company is also working on ways to implement the ECC into the efforts of the Trusted Computing Platform Alliance (http://www.trustedpc.org), a coalition of computer vendors interested in embedding stronger security functionality within computers. In these applications, the ECC can be implemented in the system's basic input/output system (BIOS) setting to insure that documents that are called up on a computer haven't been tampered with since the last authorized use. The ECC can also restore corrupted documents to their former state.

Company Profile:

GORCA Memory Systems went out of business in 1999. The intellectual property of the error correcting system was sold to SIDY. SIDY, incorporated in 1973, specializes in telecommunications systems, including intelligent call processing platforms which provide telecommunications service capabilities to the public switched telephone network. The company has recently focused on providing products for packet-based data networks. TEP has spearheaded the development of refinements to the ECC to add capabilities not available with other ECCs. TEP, working jointly with SIDY, has led the development of HEDC FEC chip which SIDY will produce and market.

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Note: The Ballistic Missile Defense Organization (BMDO) and the Strategic Defense Initiative Organization (SDIO) are predecessors of the Missile Defense Agency (MDA).

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ECC

Short for **Error-Correction Code**, **ECC** is a method of detecting and then correcting errors within the computer memory.

When purchasing computer memory you may notice ECC or NON-ECC memory, or Error-Correction Code Memory / Non-Error Correction Code Memory. Generally, NON-ECC memory will always be cheaper.

Additional help and information about computer memory can be found on our memory help page.

Also see: Memory definitions, Parity

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Parity

Basic method of checking data for errors during a transmission or on a data storage mechanism. Parity works by setting a parity bit to an even or odd number. If the binary stream contains eight 0's or 1's, for example, we know that this is an even number, however if the parity bit indicates that this number should be an odd number we would be able to easily determine that the data is corrupt.

Also see: CRC, ECC, Error control, Mark parity, No-parity, Parity bit, Parity Check, Space parity

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